

Why CMOS Image Sensors are Poised to Surpass CCDs

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Introduction

The proliferation of the next generation of imaging systems has been greatly accelerated by the implementation of Complementary Metal Oxide Semiconductor (CMOS) imagers. These devices are fabricated right alongside chips for modems, fax engines, cellular phones and microprocessors. And, with these economies of scale come subsequent cost reductions. Ever since imager chip designs have improved and design rules have shrunk to sub-micron levels resulting in increased functionality within the pixel site, the image quality of CMOS imagers can now compete with CCDs. CMOS imagers are, practically, more of an imaging system rather than just a sensor. A CMOS imager typically consists of an imaging core (similar to a CCD in that discrete signal levels are multiplexed to a single output), all of the timing logic, usually requiring only a single clock for operation, on-chip programmability of features such as gain, integration time, and windowing, and an Analog to Digital Converter. Indeed, when a designer purchases a CMOS imager, its not like buying an ECL NAND gate or a TTL SRAM, but an entire system consisting of an imaging array, logic registers, memory, timing generators, and an ADC. Imaging system integration on a chip not only has the advantage of lower power dissipation but also a smaller BOM, less required space, and overall lower cost compared to a conventional CCD imaging system.

Charge coupled device technology background

Since the early 1970's, Solid State imaging systems have primarily been utilizing Charge Couple Device (CCD) technology for the imaging component. CCDs use the inherent photoresponsiveness of silicon to convert incident photons into electrons. Implants in the silicon and voltage biases on polysilicon gates confine the generated electrons to discrete packets. These gates are then sequentially clocked and the individual packets of charge in each pixel eventually travel to an output amplifier. In an imaging 2-D array this is usually accomplished by keeping columns separate by an implant and transferring each row of data into a serial multiplexer. Once the serial multiplexer transfers a line of data to the output amplifier the next row is transferred into the serial multiplexer. The output amplifier proportionally converts the electrons into an output voltage. A CCD is an analog device. The clocks required to clock the gates often have rail voltages of various levels such as +4, -8,

-12, etc. and the output amplifier has its own set of "non-standard" DC bias levels. This architecture helps explain some of the advantages and disadvantages of CCDs as imaging devices. Because each charge packet is separated by implants and gate voltages, an excess amount of charge can spill over to adjacent potential wells. This effect is seen as blooming and takes place in the column direction. Also, the transfer of charge is not perfect. A small amount is left behind during every transfer.

On large arrays at high clock speeds this becomes noticeable and can show up as a smearing of the image. Since every charge packet is transferred to the same output amplifier the global uniformity of the image is very good, meaning the fixed pattern noise is quite low. It also means that this one amplifier must have all of the device gain and a very high bandwidth, allowing for a high white noise because every pixel in the array must be amplified within a single frame time.

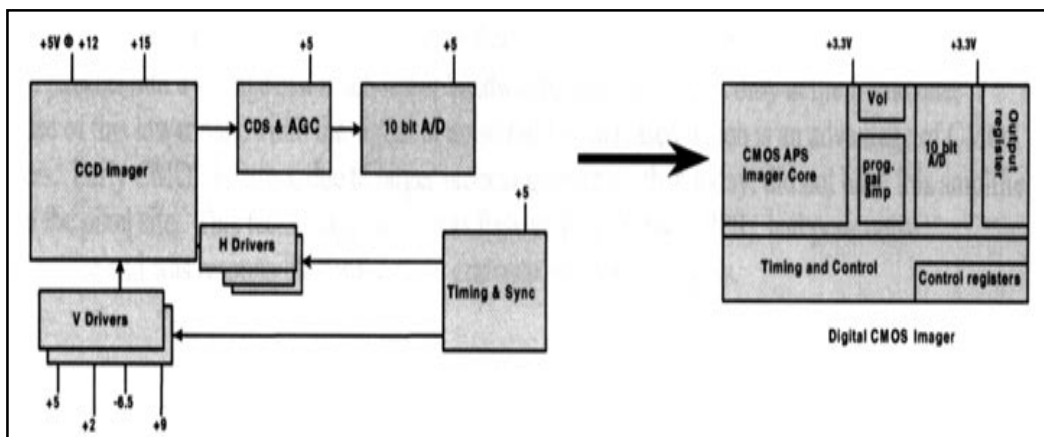


Diagram 1. CMOS offers high system integration.

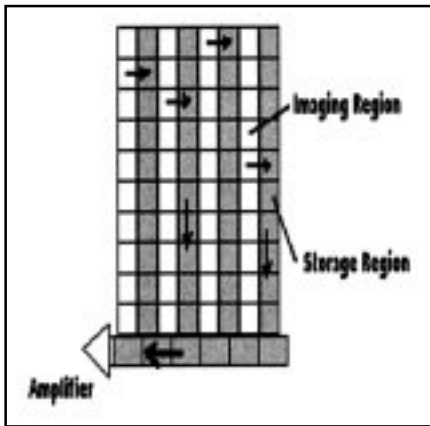


Diagram 2. CCD Array.

CMOS imager technology fundamentals

CMOS imagers on the other hand, have an amplifier within each pixel site. This converts the discrete charge packets into a voltage at a much lower bandwidth, needing to reset only at the frame rate. Because of this lower bandwidth the signal to noise ratio is increased which is an advantage of CMOS imagers. Early CMOS imagers, due to larger process geometries than today, did not have this amplifier within the pixel site. This technology, known as Passive Pixel Sensor (PPS), had poor noise performance and was responsible for the early criticism of CMOS imagers.

But today, with the decreased process

(a.k.a. fill factor) has been obviated by the use of micro-lenses; tiny lenses fabricated on each pixel site which re-directs the incident illumination that would have otherwise fallen on interconnects or transistors back to the photo sensitive diode area.

An additional advantage of CMOS imagers is the inherent anti-blooming since the charge is contained within the pixel site. The voltage that is generated within the pixel site is switched first onto a column buffer and then to the output amplifier. Since the voltage is switched directly to the output amplifier there is no loss of charge during transfer and subsequently no image smearing. The drawback is that each amplifier in every pixel has slight differences in threshold voltage creating offsets that result in fixed pattern noise. As designs and processes improve this effect has dramatically been reduced.

Due to this functional integration, many imaging applications are now

whereas another data sheet may emphasize dynamic range or full well capacity. The designer's challenge is, therefore to determine which parameters are most critical for their application and take advantage of the vast "array" of CMOS imagers available. The successful designer will find the right imager that produces great image quality for their application at a low system cost.

A few of the critical device characteristics to be concerned about with any imager are signal to noise ratio, dynamic range, noise, optical format, and voltage requirements. Important parameters to know and compare are full well capacity,

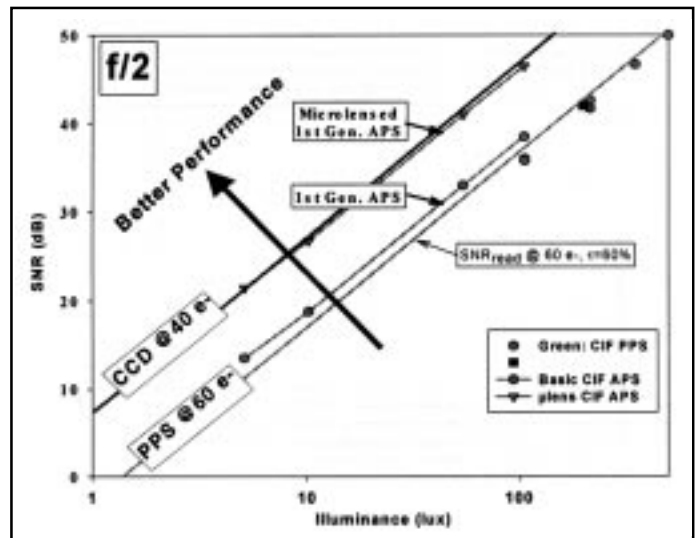


Diagram 4. Noise level to be competitive with CCDs.

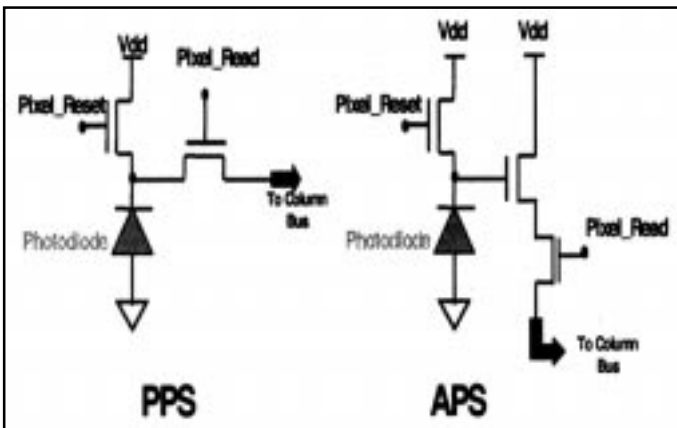


Diagram 3. CMOS imager design structure

geometries, increased pixel complexity is possible. Additional features can be added within the pixel site including electronic shutter, Trans-impedance amplifiers, and sample-and-hold circuitry to decrease fixed pattern noise. Indeed, at CONEXANT, on an advanced CMOS imager design with six transistors per pixel, read noise levels of one electron have been measured. The increased amount of circuitry within the pixel has reduced the area available for the light sensitive diode. The decrease in this ratio

feasible that would not have been practical in times past. Children's toys, more discrete security cameras, are all on some designer's drafting board.

Imaging system design considerations

However, there remains in this industry a general concern regarding the lack of standards in measurements, specifications, array sizes and characteristics. The reason is simple: each company has its own strengths and weaknesses. So, in comparing data sheets, an engineer may find one giving data on read noise or signal to noise ratio at low light levels

read noise at your operating conditions, quantum efficiency, and dark current. Other parameters, like signal to noise ratio (SNR), are derived from those basic measurements.

For low-light level applications, such as security cameras, read noise and quantum efficiency are most important. In moderate to high light level applications, such as outdoor photography, a large full well capacity is more important.

The most misunderstood and often misquoted parameters are dynamic range and signal to noise ratio. Dynamic range is the full well capacity divided by the lowest measurable read noise. It may be misleading because often times the read noise is not measured at the typical operating speed and often does not take dark current shot noise into account. Signal to noise ratio (SNR) depends upon the incident light level (at very low light levels the noise may actually be larger than the signal). SNR should take into account all noise sources. Some data sheets ignore shot noise, which is the dominant noise source at moderate to high signal levels. Instead SNR_{DARK} is specified, which is really nothing more than dy-

dynamic range. Another confusing spec is digital SNR or dynamic range, which is only the characteristic of the A/D converter. This may be important, but does not accurately describe image quality. Also keep in mind the A/D resolution may not necessarily limit imager dynamic range if the imager has multiple analog gain settings.

Optical format also confuses many

the target customer is. If the customer is the school system with established systems with Windows '95 you better make sure your imaging system does not require Win '98. If the goal is to capture and store many low-resolution images, don't specify a high-resolution imager that will provide excellent image quality but will produce more data than can be stored. There are also many non-stan-

ding imagers that address a variety of applications.

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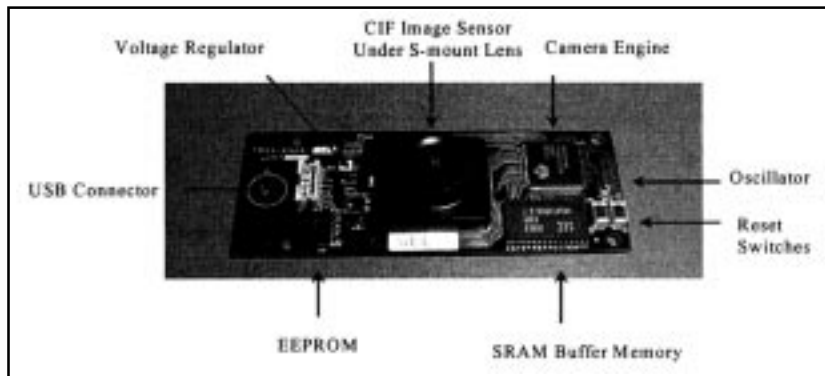


Diagram 5. CONEXANT's USB Camera Module.

because its legacy has generated an unusual definition. From the days of vidicon tubes where only part of the area produced useful imagery, the calculation includes swapping units and rounding up. By taking the diagonal dimension of the imager in millimeters and dividing by sixteen, you have the optical format in inches. However, if your answer is 0.38 your format is not 1/3 inch, its 1/2 inch. This is where the rounding up occurs. If you specify a 1/3 inch lens for such an imager, you could suffer from image vignetting (shadowing) in the corners. Data sheets sometimes cheat on this by rounding down, taking that 0.38 inch format and calling it 1/3 inch, for example. The reason is simple, 1/3 inch optics cost less than 1/2 inch optics but it may hurt system performance. The designer should perform the calculation and try various optics to get desirable performance.

A great advantage of CMOS imagers is the requirement for only a single voltage to power the device but the designer should still take care in laying out the board to power the chip. As common practice dictates, digital and analog voltages should remain as separate as possible to prevent unwanted crosstalk and, as with all good board layout, grounding and shielding are very important. Even though the imager is a CMOS device with standard voltages for the I/O, the real input signal of interest (photons) is quite small and can be susceptible to noise.

For the designer this is an exciting and challenging time. It is up to the manufacturer to define exactly what their imaging system is supposed to do and who

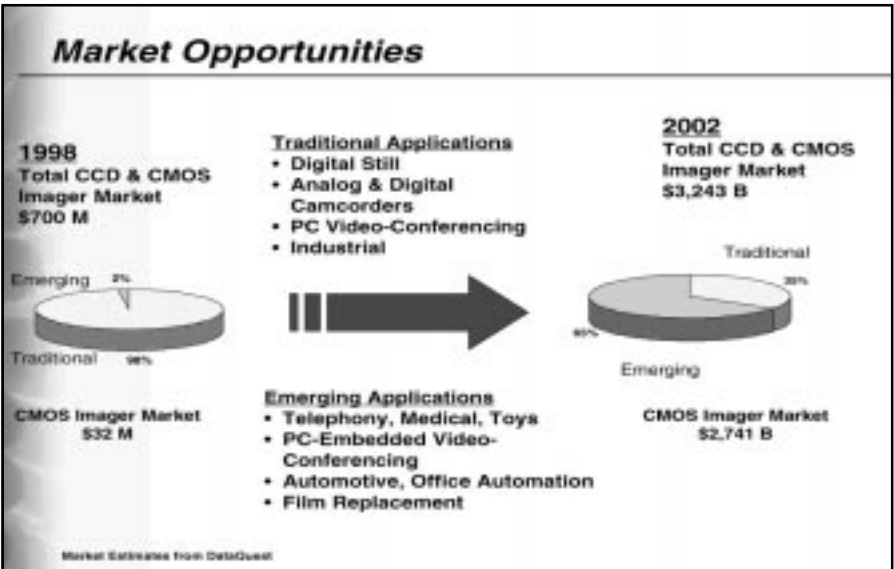
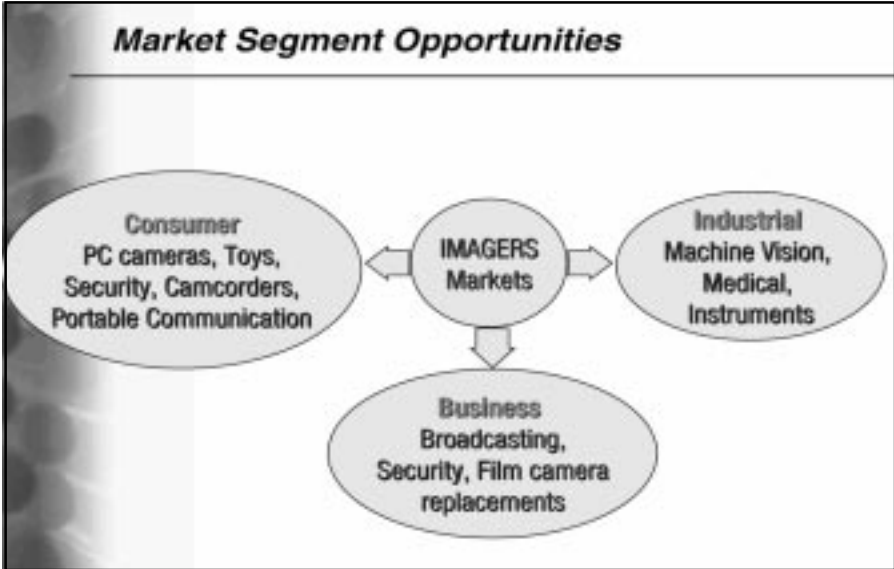
standard interfaces. There are currently several types of removable memory media for digital still cameras, including PCMCIA, Toshiba flash and even floppy disk. The most important thing is to get samples and spend up-front time evaluating performance in the environment that the product will operate in.

Potential applications

Arising from all of these CMOS imager benefits is a vast number of potential applications.

A new cellular telephone standard being implemented within the next couple of years will have sufficient bandwidth to send images along with sound. Most all phone manufacturers are planning on implementing imagers into telephones; first addressing the insurance and realtor markets and then for everyday use. More and more toys will be implementing imagers. These will likely be of low-resolution format to keep data amounts small and will interface to television. The industrial and medical imaging markets will increase in size due to the lower cost of imaging and the decreased cost of image storage and processing. Of course, the traditional imaging markets of digital still cameras and video cameras will remain strong. It is even possible to integrate the entire camera on a chip, where only an oscillator and power supply would be required with complete video (digital or analog) out of the chip. The only reason that has not been marketed yet is due to its limited market potential due to such specialization. All imager manufacturers at this time are concentrating on pro-

Presentation Materials

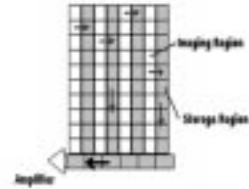


CMOS vs. CCD Imagers

<ul style="list-style-type: none"> • CMOS Technical Advantages <ul style="list-style-type: none"> • Standard processing • Functional integration • Inherent Anti-blooming • Low Temporal Noise • Single voltage requirement Market Advantages <ul style="list-style-type: none"> • Lower total system cost • Greater levels of integration leveraging new standards - USB, Firewire 	<ul style="list-style-type: none"> • CCD Technical Advantages <ul style="list-style-type: none"> • Uniform output • Low Spatial Noise Market Advantages <ul style="list-style-type: none"> • Market momentum • Known capabilities
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CCD Characteristics/Shortcomings

- Light (photon energy) hits the imaging region, causing a charge to build up at each pixel.
- If a pixel is exposed to too much light the charge can overflow onto adjacent pixels. This can cause the phenomenon known as blooming, and appears as horizontal or vertical streaks.
- During integration, the charges are transferred in a parallel-serial fashion to the output amplifier.
- The output amplifier must have high gain-bandwidth to reset for every pixel per frame so large amounts of white noise are also amplified.



CCD Array

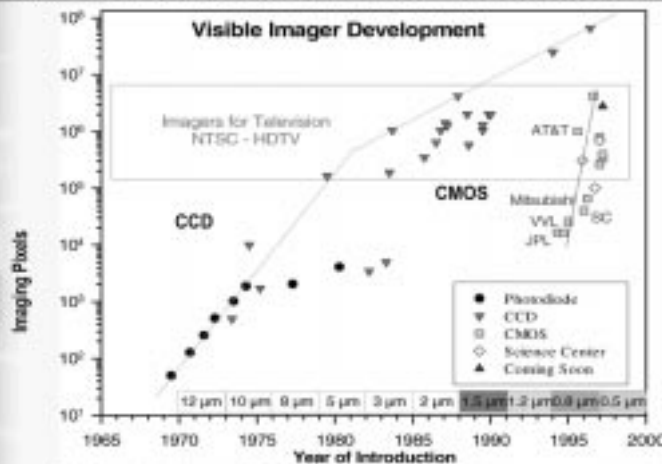
CMOS Offers High System Integration



Typical CCD imaging system

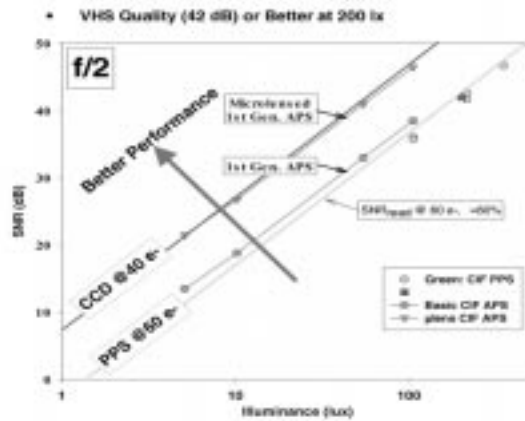
Equivalent Conexant CMOS single-chip imaging system

CMOS Performance that Competes with CCDs



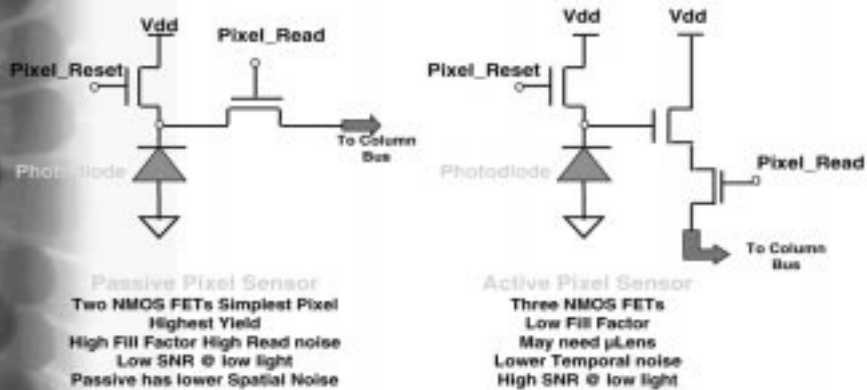
Sub-μm CMOS enables better CMOS imager performance that now competes with CCDs

Noise Level to Compete with CCDs

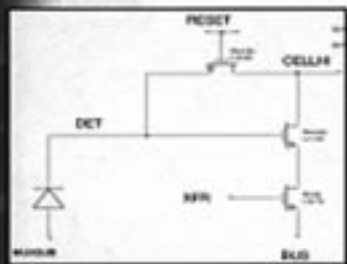


Active Pixel Sensor design and microlenses enable CMOS imagers to compete with CCDs

CMOS Imager Design Structure



5.6 μ m 3T Active Pixel Sensor

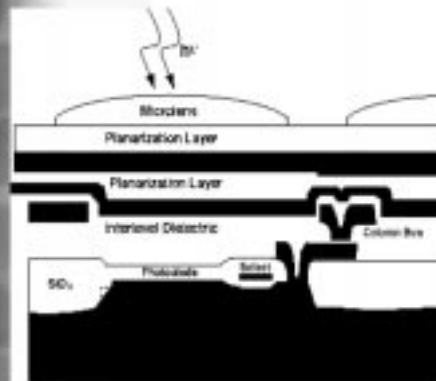


Fill Factor is the percentage of pixel area that is light sensitive: It is effectively increased with microlenses



26% Optical Fill Factor using Rockwell's 0.5 μ m Lithography.

CMOS Imager Pixel Profile



- Silicon process is followed by color filter deposition and then microlens deposition
- Smaller process geometries enable amplification within the pixel decreasing noise bandwidth to increase SNR
- Further processing advances will lead to even greater levels of performance and functional integration

Imager Design Considerations

Signal-to-Noise Ratio (SNR)

- Definition
 - "Maximum signal divided by total noise from all sources"
- Amplifier noise dominates at low light levels
- Dark current shot noise dominates at high temperature
- Shot noise dominates with moderate and high signal levels
- Conexant's SNR is nominally 48dB, which is in line with industry standards

CMOS Imager Design Considerations

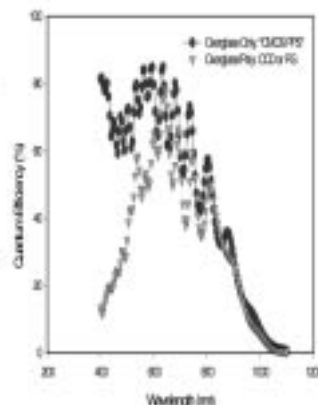
Dynamic Range

- Definition
 - "Maximum signal capacity divided by lowest read noise" or "Full charge capacity range available for signal"
- Often confused with Signal-to-Noise ratio
- Specified in dB or as a ratio
- Conexant's measured dynamic range is 60dB which is above the typical industry standard

CMOS Imager Design Considerations

Quantum Efficiency

- Definition
 - "Ratio of electron/hole pairs generated for each incident photon"
- Factors
 - Starting material
 - Light absorbing layers above detector (Photodiode beats Photogate)
- Conexant's Quantum Efficiency exceeds normal industry standards.

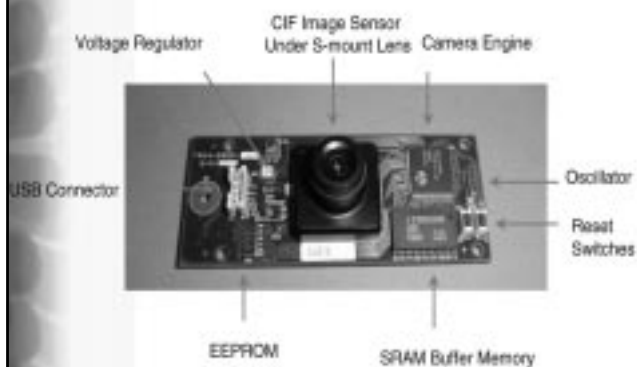


CMOS Imager Design Considerations

Optical Format

- Definition
 - Optical Format in inches is defined as the imager's diagonal measurement in mm divided by 16.
- Defined during the vidicon years
- Imager Optical Format must be less than lens Optical Format to avoid vignetting
- Increased Imager size increases cost of Imager and Optics; it also increases device sensitivity

USB Camera Module Reference Design



Conclusions

- CMOS imager design is now sufficiently mature to technically compete with CCDs.
- Functional integration results in lower system cost and power dissipation.
- Designers can take advantage of proliferation of imagers but need to carefully analyze device characteristics.
- CCDs are holding on to market share. However after evaluating all design considerations, CMOS imagers are the future.